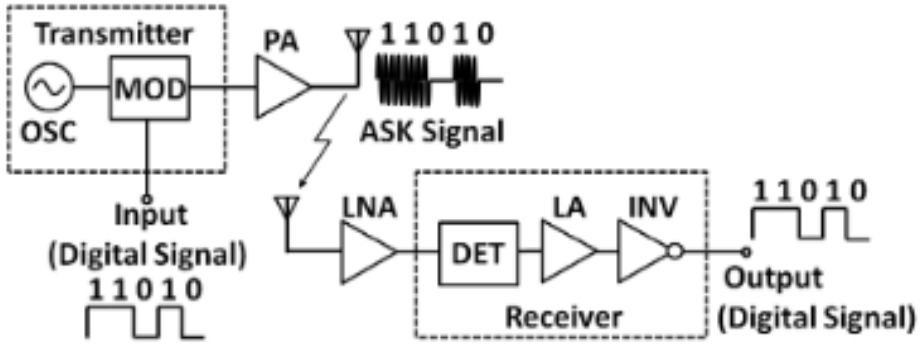
Master/Bachelor Thesis/Hiwi
Exploration of ASK receiver at 60 GHz with 10 GHz of bandwidth for higher data rate

Background:

To achieve a high data rate and low power consumption, ADCs, DACs, and PLLs are avoided. An amplitude shift keying (ASK) modulation method can be realized using simple circuits with low power consumption. 60 GHz band have been developed with 9 -10 GHz bandwidth. Hence, the task is to explore the maximum data rate for ASK-based transceiver at 60 GHz with the available bandwidth.



Block diagram of transmitter and receiver

Tasks of receiver at 60 GHz:

To set up ASK receiver in Cadence 65 nm CMOS technology.

Phase 1: Research Literature
- Make a survey on ASK demodulation.
- Study of LNA, detection, limiting amplifier and inverter.

Phase 2: Receiver modeling and Circuit Design
- System level modeling of receiver in Verilog AMS.
- Detector and inverter IC design.

Phase 3: Evaluation
- Evaluation of the receiver performance.
- Thesis and publication.

Further information on this and other topics could be delivered by email, telephone or discussion.

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