Master/Bachelor Thesis/Hiwi
System-Level Modelling and Simulation of Transceiver Base Continuous Phase-FSK

Background:

CPFSK is chosen because of its attractive function for modulation in modern short-range wireless systems. Its implementation complexity is low, resulting in low-power consumption and its availability to the implementation up to THz-frequencies.

Tasks:

To set up the high data rate (>10 Gbps) transceiver simulation chain in Cadence based on Verilog/Verilog AMS.

Phase 1: Research Literature

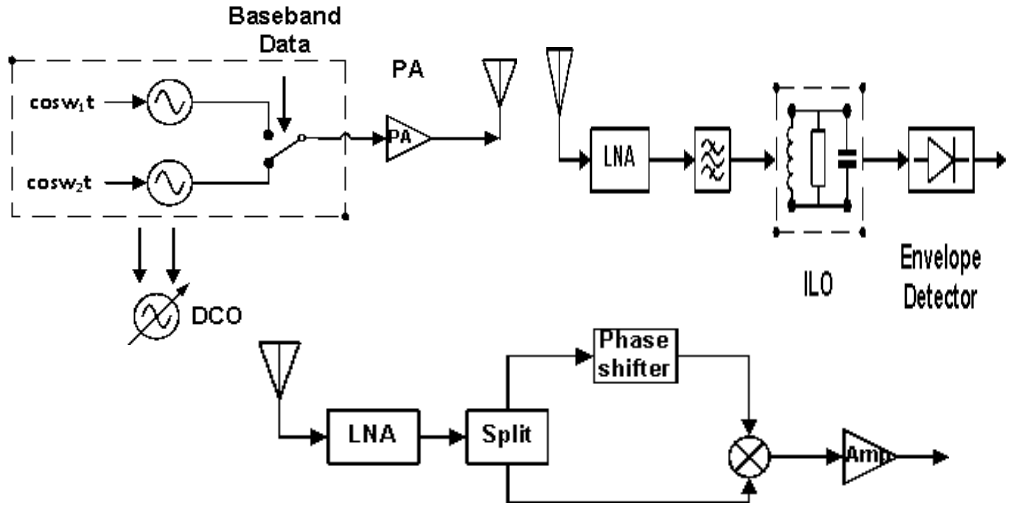
- Make a survey on CPFSK modulation and demodulation.
- Study of VCO, DCO, PA, LNA, filter function.
- Understanding of the whole transceiver parameters.

Phase 2: Modeling and simulation

- Study of Verilog/Verilog AMS
- Transceiver modeling and simulation at 60 GHz.

Phase 3: Evaluation

- Evaluation of the transceiver performance (data rate, bandwidth efficiency)



Block diagram of transmitter and receiver

- Energy evaluation of transmission system.
- Thesis and publication.

Further information on this and other topics could be delivered by email, telephone or discussion.

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