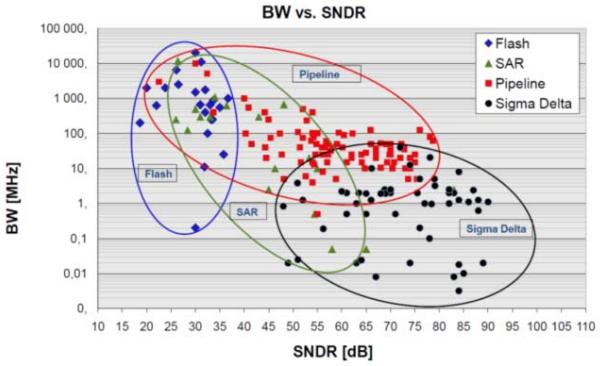
Master Thesis

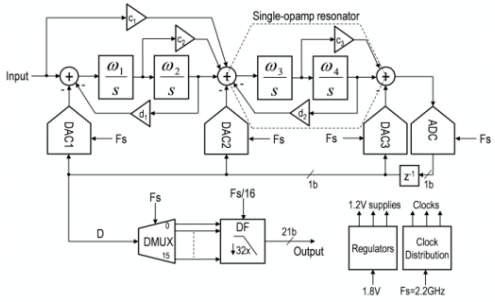
Design of 12 bits wideband ADC for 5G

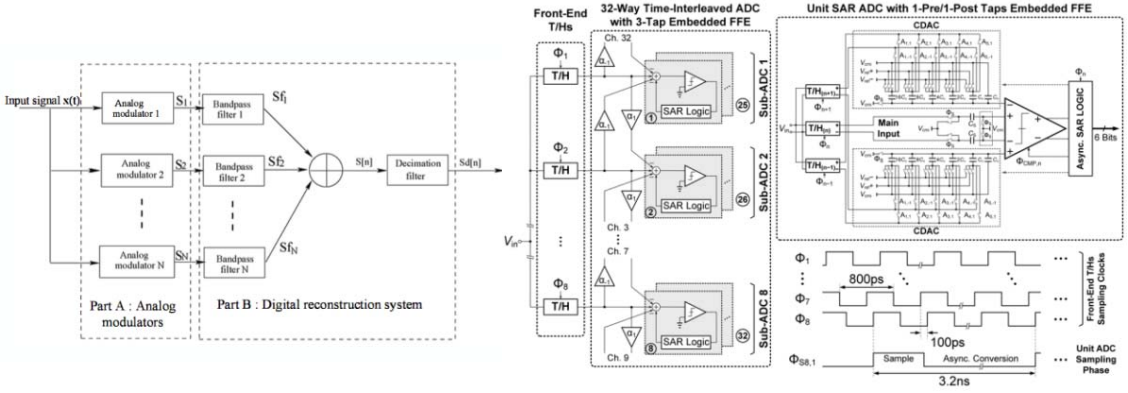
Background:

The increasing demand on integrated high data rate communication standards is pushing for high linearity / high sampling rate / wide bandwidth circuits. High speed / High resolution data converters (ADC's and DAC's) are crucial blocks to build such communication systems.

The main challenge in this topic is to design a state-of-the-art 12 bits ADC with 5GHz sampling frequency and 1 GHz bandwidth in a 65nm standard CMOS technology with competitive power consumption. Many approaches are used to realize such ADC either by combining different topologies or by using cascading of certain toplogy.







ADC FOM and Wideband ADC Implementation Examples

Tasks: (The tasks can be divided into three main milestones)

1.Literature survey and behavioral modeling **(9 weeks)**

- Comparing the state-of-the-art published ADC's
- Finding the suitable toplogy to implement the ADC
- Applying the top-down design methodology by building behavioral models for the complete system to make proper noise/power budget allocation for the building blocks
- Make a 1st design review

2.Circuit design implementation **(7 weeks)**

- Circuit design in Cadence using the TSMC 65nm technology
- Make the 2nd design review with all circuit schematics

3.Verifications and documentation **(8 weeks)**

- Applying the bottom-up verification by doing the layout design of critical blocks and post layout verification
- Make the final design review
- Documentation (thesis & publication)

Further information on this and other topics could be delivered by email, telephone or discussion.

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