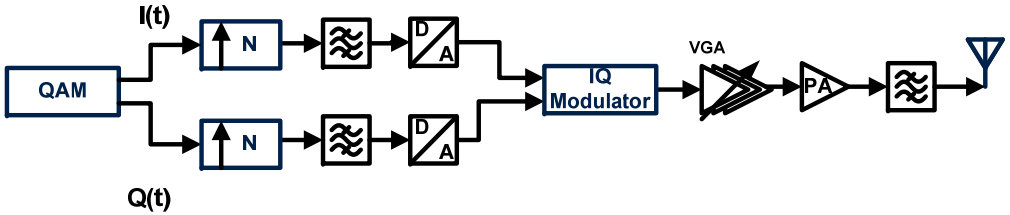
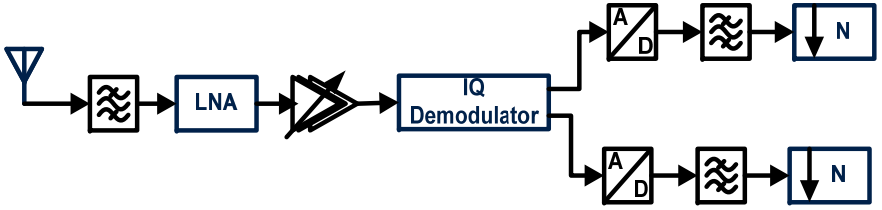
Diploma/Master/Bachelor Thesis/Hiwi
System-Level Modelling and Simulation of High Data Rate Transceiver



Block diagram of transmitter



Block diagram of receiver

Background:

Key objectives of the project are concepts for transceiver operating at 60 GHz in a bandwidth between 1-10GHz. We aim to design a wireless transmission system for data rate beyond 100Gb/s, which includes the support of high modulation orders and multi-antenna transmission. The choice of baseband architecture can have a large impact on the overall system complexity and power consumption of the tranceiver. Meanwhile, setting up the transceiver simulation chain in Cadence has an absolute advantage for the verification of highly complex systems. Hence, we choose modeling the system level of transceiver in Cadence with Verilog/Verilog AMS.

Tasks:

To achieve the key objectives, the following goals should be met, namely:

- ❖ Study of the whole transceiver structure.
- ❖ Modeling the transmitter and the receiver in Cadence with Verilog/Verilog AMS.
- ❖ Study of analysis in Matlab, such as he transmitter output spectrum and adjacent channel leakage ratio (ACLR).
- ❖ Energy evaluation of transmission system.

Further information on this and other topics could be delivered by email, telephone or discussion.

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