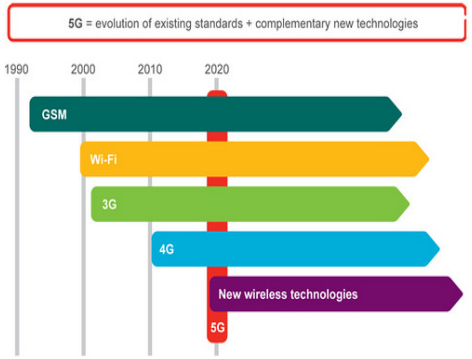
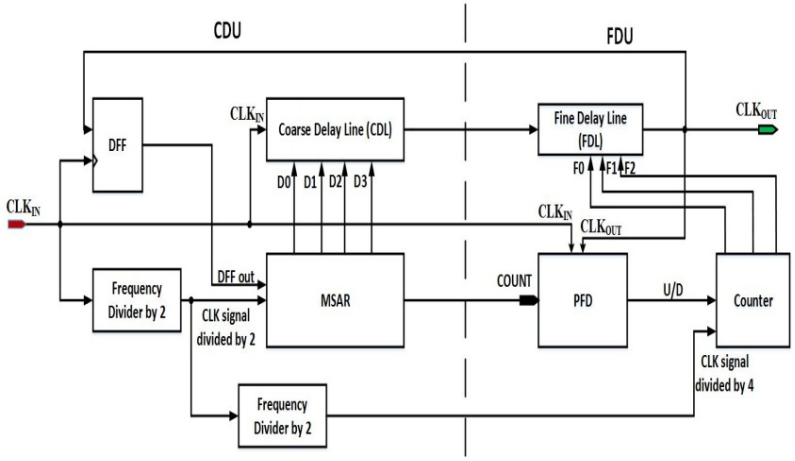
Master Thesis
All-Digital Delay Locked Loop with Edge Combiner in 65nm CMOS for 5G standard



Evolution of 5G standard



General block diagram of ADDLL designed in 130nm

Background:

As the technological development in semiconductor technology increases rapidly, microprocessors become more and more complicated so this will lead a bigger chip size since more Integrated Circuits (IC) blocks are integrated into the same chip and higher operating frequency that enables high speed operations. As the chip becomes more complicated, keeping it in optimal operating condition and preventing any malfunction problem also becomes much more difficult. One of the biggest challenge in the design is clock signal distribution. Since all blocks in the chip is driven by the same clock signal, Internal clock signal generated by the local oscillator has to be exactly the same for all parts of the chip to avoid synchronization problem. If there is a delay difference between their clock signal, they can miss their correct state and that causes a big performance degradation in overall performance and the circuit can not work correctly. This phenomena is called clock-skew problem.

Tasks:

For this work, we will use the ADDLL structure in 130 nm developed by HFE to design new DLL in 65 nm to reach much higher frequency and better phase noise and jitter performance at targeted frequency.

The target frequency range is between 18 to 28 GHz for 5G standard. The total duration of the thesis will be six months and the student will get to have hands-on experience on state of the art industrial experience on Cadence Design Environment tools.

Further information on this and other topics could be delivered by email, telephone or discussion.

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