Bachelor/Master Thesis
Design of a high speed RF-DAC based Transmitter

Background:

In our research group at HFE we are designing integrated transceivers for mobile communication devices. The mobile communication standards follow the trend of increased data-rate. Therefore, we have two options namely increasing the modulation order or increasing the bandwidth. The modulation order is limited by the noise performance and the sensitivity of the blocks. And bandwidth is a finite resource especially within the congested frequency range of the mobile communication standards. Therefore, we are going to high frequencies such as 60GHz where a bandwidth of 2 GHz is possible.

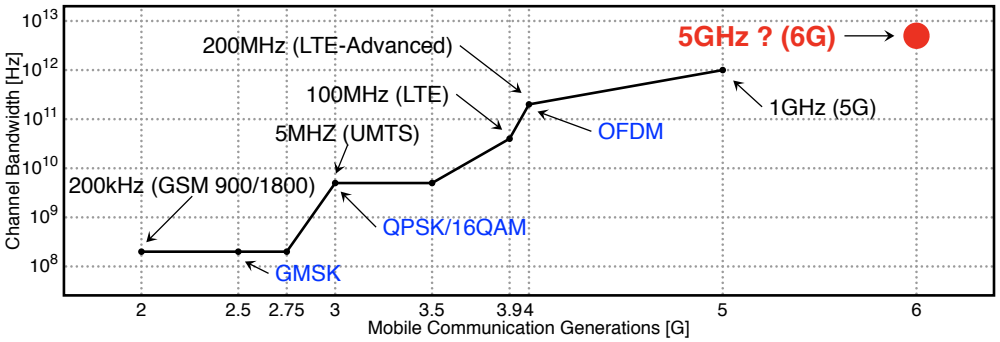
Considering the increased bandwidth the RF-DAC must switch at a very high frequency. If one takes into account the digital signal processing which contains oversampling and filtering the RF-DAC must achieve a sampling rate of several GS/s.

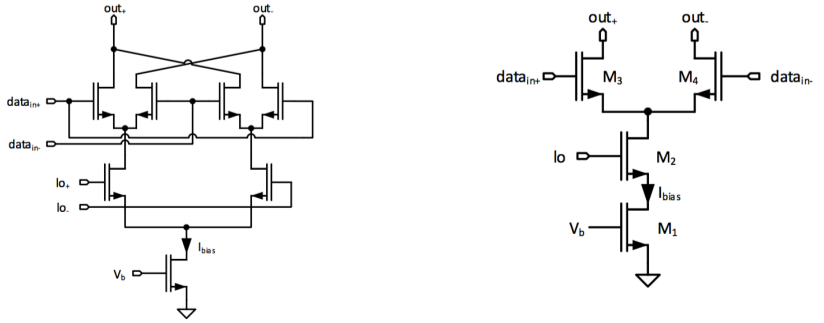
Tasks:

The tasks can be divided into three different blocks.

1. Literature research
   - Finding suitable RF-DAC topologies for such high sampling rates
   - Modelling of several RF-DAC topologies for further investigations
2. Implementation
   - Circuit design in Cadence using the TSMC 65nm technology
   - Layout of critical blocks
3. Verifications and documentation
   - Verify the circuit (Postlayout simulations)
   - Documentation (thesis)

Evolution of Bandwidth in Mobile Communication Standards





Examples for different RF-DAC cells

Further information on this and other topics could be delivered by email, telephone or discussion.

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