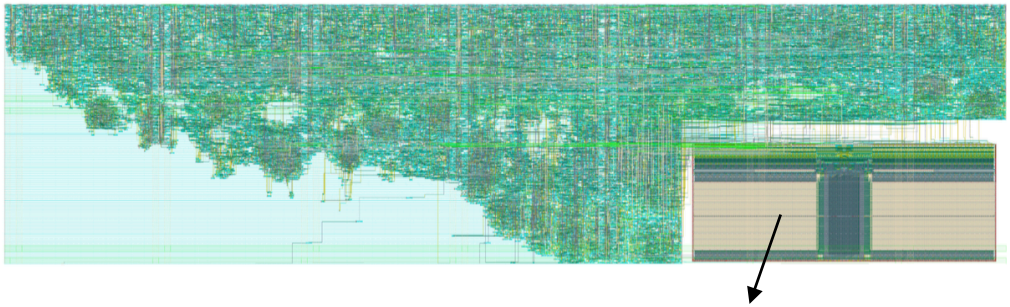
Bachelor/Master Thesis
Design of a high speed serial interface for chip to FPGA / FPGA to Chip communication for a Transceiver

Background:

In our research group at HFE we are designing integrated transceivers for mobile communication devices. The mobile communication standards follow the trend of increased data-rate. Therefore, we have two options namely increasing the modulation order or increasing the bandwidth. The modulation order is limited by the noise performance and the sensitivity of the blocks. And bandwidth is a finite resource especially within the congested frequency range of the mobile communication standards. Therefore, we are going to high frequencies such as 60GHz where a bandwidth of 2 GHz is possible.

Testing the transceivers requires a high speed computer interface since the baseband processing takes place in Matlab. This allows us maximum level configurability. The interface can be used to transfer data slowly onto a SRAM memory on chip during the setup mode which can be read very fast during the transmit mode. This interface is additionally used to set up the analog and digital blocks during the start-up of the chip.



Synthesized UART interface and digital frequency generation

Tasks:

An appropriate UART based interface and a memory controller is already implemented. The task of the student is to understand the function of the blocks. And implement additional functions such as a debug mode which makes it possible to send debug information from analog and digital blocks on the chip to the FPGA. Furthermore a receive mode for the chip must be implemented which can store the demodulated data on the memory and send them later to the computer. The blocks will be implemented using Verilog/VHDL simulated using ModelSim and Cadence. Afterwards the blocks will be synthesized for the FPGA and the chip using TSMC 65nm technology.

Further information on this and other topics could be delivered by email, telephone or discussion.

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