Master Thesis
Time-to-Digital Converter (TDC) based all-digital PLL in 65nm CMOS

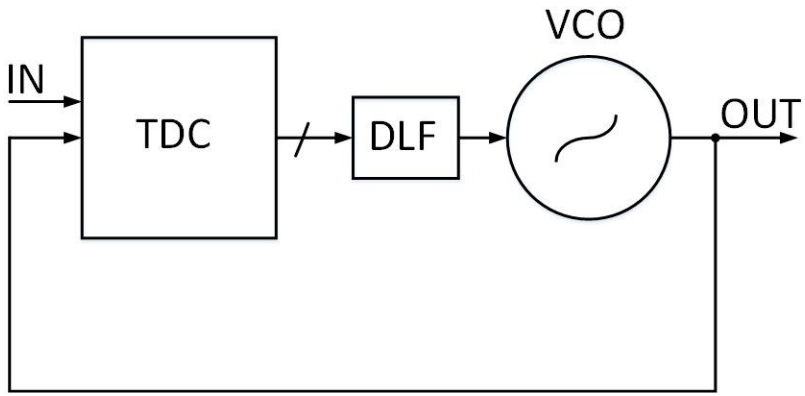
Background:

As the technological development in semiconductor technology increases rapidly, microprocessors become more and more complicated so this will lead a bigger chip size since more Integrated Circuits (IC) blocks are integrated into the same chip and higher operating frequency that enables high speed operations. Thus, PLL is one of the most important component in the system to create the required frequency. There are several techniques to replace conventional analog PLL. Time-to-digital converter is one of these techniques which replaces the analog part of PLL. However, techniques like vernier delay line and time amplifiers in TDC are power hungry and occupy large area. That's why, in this design, ADC based TDC is proposed to overcome the resolution and power consumption problem of conventional TDC methods.The advantage of this system unlike conventional PLL, it does not use frequency divider which is the one of the main contributer to the output phase noise.

Tasks:

For this work, we will use TDC structure to design all-digital PLL in 65 nm CMOS to reach high frequency with good phase noise and jitter performance.

First of all, modelling will be done with matlab simulink to determine the overall structure and critical design parameters. Then, schematic and layout parts will be done with Cadence.



General block diagram of TDC based ADPLL in 65nm CMOS

Further information on this and other topics could be delivered by email, telephone or discussion.

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