Master Thesis topic
Efficiency enhancement of class-O power amplifiers at back off power

The power added efficiency (PAE) of a power amplifier (PA) is calculated as:

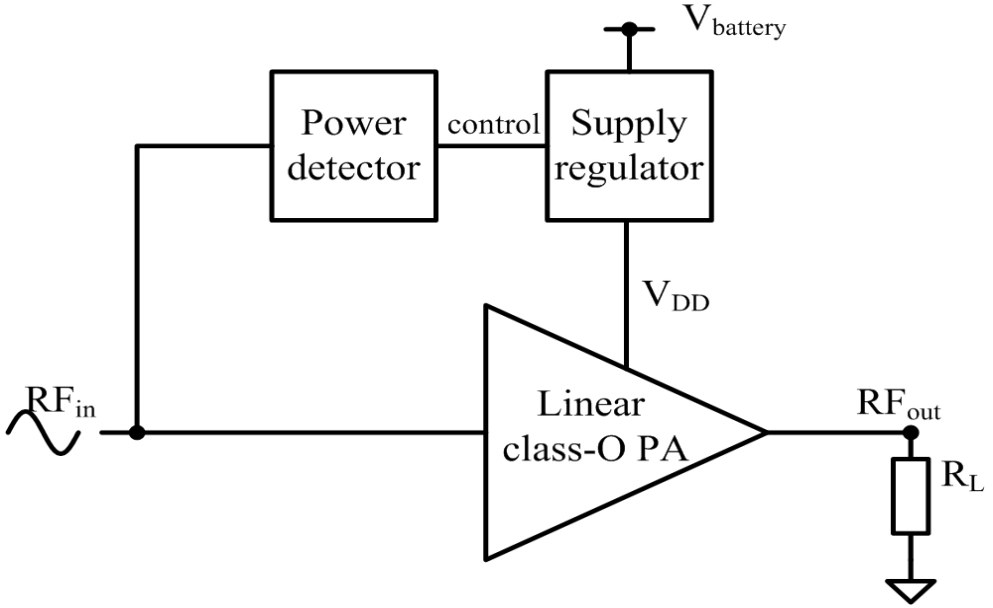
$$PAE = \frac{P_{RF}(o)}{P_{DC} + P_{RF}(i)}$$

$$P_{DC} = V_{DD} * I_{DC}$$

Class-O PA, developed by HFE, is highly linear and satisfies the LTE linearity requirements. Its efficiency is high at peak power. It is required to provide a system capable of achieving a high efficiency when the output power is backed off.

At low power, $P_{RF(o)}$ is low. When V_{DD} is kept high, the efficiency is very small. Scaling the supply voltage down using DC/DC converter at low output power, improves the efficiency at back off significantly. This can be achieved using low dropout (LDO) voltage regulators. A power detector is necessary to provide a control voltage to adapt the supply voltage of the PA depending on the RF input signal.

Task description:
- System modelling and simulation using the implemented class-O prototype and ideal components
- Implementing a PCB of the system using off-shelf components
- Verifying the overall performance of the implementing board consisting of the class-O chip and the commercial power detector and LDO components



Class-O power amplifier system with back off efficiency improvement

Further information on this and other topics could be delivered by email, telephone or discussion.

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